REMARKS

Claims 1-23, 47 and 49-51 are pending in the present application. Claims 1, 17 and 47 have been amended. Claim 48 has been canceled.

Claim Rejections-35 U.S.C. 102

Claims 1-7, 10-23 and 47-51 have been rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Application Publication No. 2005/0046002 to Lee et al. (hereafter "Lee"). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The present application is a U.S. national stage application of International Application No. PCT/JP2004/011454 which has an international filing date of November 21, 2005. The publication date of Lee in contrast is March 3, 2005. Lee thus does not qualify as statutory prior art under 35 U.S.C. 102(b). This rejection is thus improper for at least these reasons.

Moreover, the stacked semiconductor device of claim 1 includes in combination among other features a first insulating layer "for covering said first insulating material layer of said first multilayer wiring part and provided over the first main surface of said first semiconductor substrate, said first insulating layer is a support member of said first semiconductor substrate"; and a second insulating layer "for covering a second main surface of said first semiconductor substrate that is opposite the first main surface of said first semiconductor substrate, wherein the first insulating layer has greater

thickness than the second insulating layer."

As shown in Fig. 1 of the present application, the stacked semiconductor device includes a first semiconductor device 2 having a first insulating layer 8a formed on a main surface of first semiconductor substrate 6a, and a second insulating layer 11a formed on a rear surface of first semiconductor substrate 6a. Moreover, a thickness of first insulating layer 8a is greater than a thickness of second insulating layer 11a. For example, the thickness of first insulating layer 8a may be about 200 – 100 μm as described in paragraph [0032] of the application, and the thickness of second insulating layer 11a may be about several to 10 μm as described in paragraph [0035] of the application. Due to this configuration, sufficient strength and insulating properties are realized, while at the same time the total thickness of the stacked semiconductor device is minimized.

In contrast, chip stack package 100 in Fig. 3 of Lee includes encapsulating material 41 formed on both the main and rear surfaces of semiconductor chip 11. There is no disclosure or description that the thickness of insulating material 41 formed on the main surface of semiconductor chip 11 in Fig. 3 of Lee is greater than the thickness of insulating material 41 formed on the rear surface of semiconductor chip 11.

In particular, on page 3 of the current Office Action dated March 18, 2010, the Examiner has reproduced Fig. 3 of Lee as including Device A, Device B and Device C designated by the Examiner. For instance, insulating material 41 formed between Device A and Device B in the reproduced figure on page 3 of the current Office Action

may be considered as corresponding to a first insulating layer of Device A. Moreover, insulating material 41 formed between Device A and the common substrate in the reproduced figure may be considered as corresponding to a second insulating layer.

However, these corresponding portions of insulating material 41 in the reproduced figure on page 3 of the current Office Action do not meet the above noted features of claim 1, wherein the first insulating layer has greater thickness than the second insulating layer. Lee as relied upon thus fails to meet the features of claim 1. Applicant therefore respectfully submits that the stacked semiconductor device of claim 1 distinguishes over the prior art as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1-7 and 10-16, is improper for at least these reasons.

The semiconductor device of claim 17 includes in combination among other features that "the first insulating layer has greater thickness than the second insulating layer". Claim 47 includes somewhat similar features.

Applicant respectfully submits that Lee as relied upon does not include first and second insulating layers as featured in the claims, whereby the first insulating layer has greater thickness than the second insulating layer. Lee thus fails to meet the features of respective claims 17 and 47. Applicant therefore respectfully submits that the semiconductor devices of respective independent claims 17 and 47 distinguish over the prior art as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 17-23, 47 and 49-51, is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claims 8 and 9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of U.S. Patent Application Publication No. 2002/0030266 to Murata et al. (hereafter "Murata"). Applicant respectfully submits that Murata as secondarily relied upon does not overcome the above noted deficiencies of Lee as primarily relied upon, and that this rejection of claims 8 and 9 is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of three (3) months to September 18, 2010, for the period in which to file a response to the outstanding Office Action. The required fee of $1110.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.

Andrew J. Telesz, Jr.
Registration No. 33,581

11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740